MP5061

4.5V-28V Current Limit Switch with Low $R_{DS(ON)}$, Current Monitoring, and Soft Start

DESCRIPTION

The MP5061 is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output. At start-up, the slew rate at the output limits the inrush current. An external capacitor at the SS pin controls the slew rate.

The maximum output load is current-limited using a sense FET topology, in which a low-power resistor from the ISET pin to ground controls the magnitude of the current limit. An internal charge pump drives the gate of the power device, allowing for a power FET with a very low on resistance of 7mΩ.

The MP5061 includes an IMON option to produce a voltage proportional to the current through the power device, as set by a resistor from the IMON pin to ground.

Fault protections include current-limit protection, thermal shutdown, under-voltage protection, and damaged-MOSFET detection. Both the current limit and thermal shutdown have programmable auto-retry and latch-off mode.

The MP5061 is available in a QFN-22 (3mmx5mm) package.

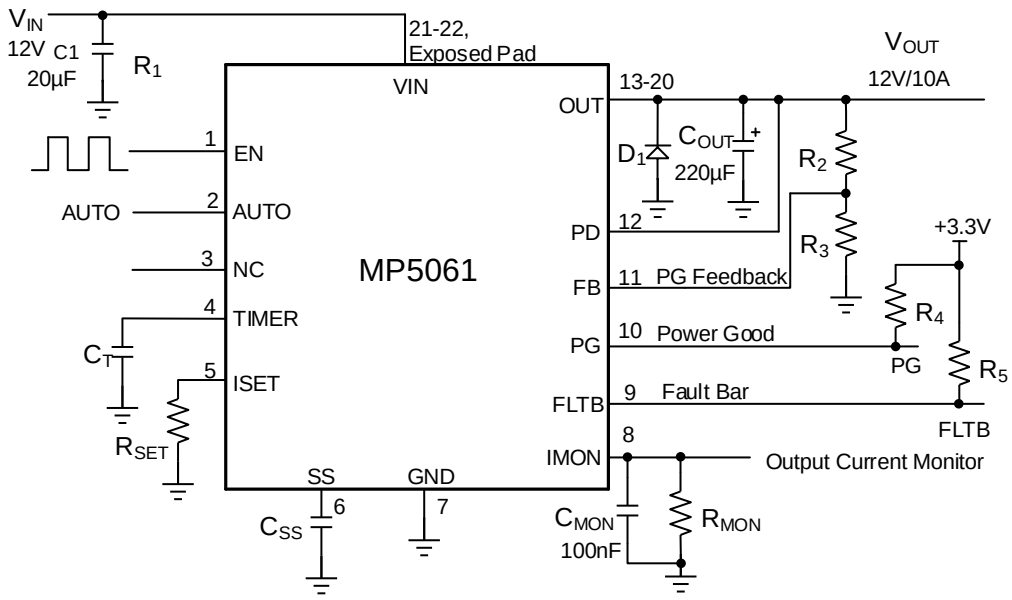
FEATURES

- Integrated 7mΩ Power FET
- Adjustable Current Limit (5A to 15A)
- 36V Input Transient before VOUT Start-Up
- Output Current Measurement
- ±10% Current Monitor Accuracy
- Fast Response (<200ns) for Short Protection
- PG Detector and FLTB Indication
- PG Assert Low at V_{IN} = 0
- Damaged MOSFET Detection
- External Soft-Start
- Under-Voltage Lockout
- Thermal Protection
- Small QFN-22 (3mmx5mm) Package

APPLICATIONS

- Hot Swap
- PC Card
- Storage Drives
- Laptops, Desktop, Monitor Add Power Accessories

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5061GQV	QFN-22 (3mmx5mm)	*See Below*

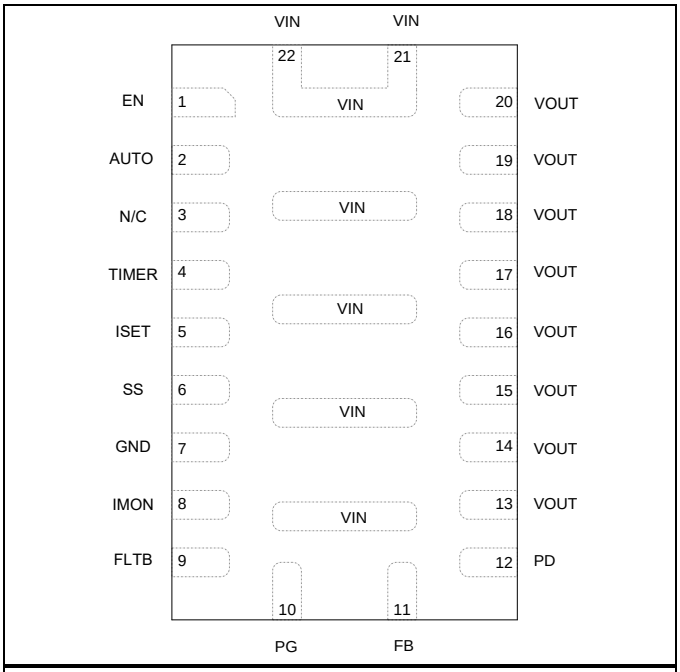
* For Tape & Reel, add suffix –Z (e.g. MP5061GQV–Z).

TOP MARKING

MPYW
5061
LLL

MP: MPS prefix
Y: Year code
W: Week code
5061: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-22 (3mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable input.** Pull the EN pin above its threshold enable the chip. Pull it below the threshold to shut down the chip.
2	AUTO	**Auto reset enable.** Float to enable auto-reset upon fault removal. Ground for the part to latch off when a fault occurs.
3	NC	**Not connected pin.** Float this pin in the application.
4	TIMER	**Timer set.** An external capacitor sets the hot-plug-insertion time delay, fault timeout period, and restart time.
5	ISET	**Current limit set.** Place a resistor to ground to set the value of the current limit.
6	SS	**Soft start.** A connected external capacitor sets the soft-start time of the output voltage. The internal circuit controls the slew rate of the output voltage at turn-on. Float this pin to set the soft-start time at its minimum of 1ms.
7	GND	**Ground.**
8	IMON	**Output current monitor.** Provide a voltage proportional to the current flowing through the power device. Place a resistor to ground to set the gain. Floating this pin is not recommended.
9	FLTB	**Fault bar.** FLTB is an open-drain output that drives to ground when an over-current or a thermal shutdown occurs. Pull up to an external power supply through a 100kΩ resistor.
10	PG	**Power good.** PG is an open-drain output. Pull up to an external power supply through a resistor. High indicates power good. Low indicates that the output is outside the UVLO window. PG starts to work when the pull-up supply is enabled, even if VIN and EN are still disabled.
11	FB	**Feedback.** An external resistor divider from the output sets the output voltage where the PG pin switches. The rising threshold is 0.6V with 65mV hysteresis.
12	PD	**Output discharge.** Connect to the output to provide a 500Ω load to discharge the output when V_{IN} is lower than its UVLO or EN is between 0.6V and the rising threshold. NC disables this function.
13-20	OUT	**Output.** Voltage controlled by the IC. Place a Schottky diode between the OUT pin and GND pin.
21-22, Exposed Pads	VIN	**Input power supply.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +36V
OUT, PD ..... -0.3V to +30V
FB ..... -0.3V to +3.3V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2) 2.7W
Power dissipation (T_A = +25°C, 10ms single pulse) 215W
Maximum current (T_A = +25°C) 25A
Storage temperature ..... -65°C to +155°C
Operating temperature ..... -40°C to +150°C

Recommended Operating Conditions

Input voltage operating range ..... 4.5V to 28V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (3) θ_{JA} θ_{JC}

QFN-22 (3mmx5mm)	46	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7 4-layer board. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, R_{SET} = 10kΩ, C_{OUT} = 220µF, T_J = -40°C to +125°C (4), typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	EN = high, no load		1	2	mA
		Fault latch off		0.7	1.2	mA
		EN = 0, V_{IN} = 12V		1	5	µA
Power FET						
On resistance	R_{DS_LS}			7	12	mΩ
Off-state leakage current	I_{OFF}	V_{IN} = 28V, EN = 0V, OUT = 0V, T_J = 25°C			1	µA
Thermal Shutdown						
Shutdown temperature (5)	τ_{STD}			167		°C
Hysteresis	τ_{HYS}	Auto-retry mode only		28		°C
Under-Voltage Protection						
Under-voltage lockout threshold	V_{UVLO_R}	UVLO, rising threshold		4.15	5.5	V
	V_{UVLO_F}	UVLO, falling threshold	2.7	3.8	5	V
UVLO hysteresis	$V_{UVLOHYS}$			250		mV
AUTO Pin						
Low-level input voltage	V_{AUTOL}	Latch-off mode			1	V
High-level input voltage	V_{AUTOH}	Auto-retry mode	2.5			V
Soft Start						
SS pull-up current	I_{SS}	I_{SS} changes with input	3	6	9	µA
Current Limit						
Current limit at normal operation	I_{Limit_NO}	R_{SET} = 10kΩ	10.5	12.5	14.5	A
Current monitor accuracy	I_{MONACC}	5A < I_{OUT} < 10A	-10		+10	%
Current limit response time (5)	τ_{RC}	I_{Limit} = 3A, add 3Ω load		20		µs
Secondary current limit (5)	I_{LimitH}	Any value of R_{ISET}		25		A
Short-circuit protection response time (5)	τ_{SC}			200		ns
Timer						
Upper threshold voltage	V_{TMRH}		1	1.23	1.4	V
Lower threshold voltage	V_{TMRL}	Over-current restart cycles	0.09	0.20	0.35	V
Fault restart duty cycle	V_{FAULT}		0.1	0.25	0.5	%
Insertion delay charge current	I_{INSERT}		15	40	60	µA
Fault detection charge current	I_{FLTD}		80	200	300	µA
Fault restart sink current	I_{FLTS}		0.15	0.5	0.8	µA
Discharge R_{ON}	R_{FLTE}	I_{OUT} < I_{Limit}	15	35	80	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{SET} = 10kΩ, C_{OUT} = 220µF, T_J = -40°C to +125°C (4), typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable						
Rising threshold	V_{ENRS}		1.4	1.8	2.2	V
Falling threshold	V_{ENFS}		1.2	1.6	2	V
Hysteresis	V_{ENHYS}			200		mV
FB (Power Good Feedback)						
Feedback rising threshold	V_{FBH}		0.51	0.6	0.69	V
Feedback falling threshold	V_{FBL}		0.45	0.54	0.63	V
Hysteresis	V_{FBHYS}			60		mV
Fault Bar/Power Good						
Low-level output voltage	V_{OL}	Sink current 1mA		0.1	0.3	V
Off-state leakage current	I_{FLT_LKG}	V_{FLTB} = 5V			1	µA
Fault bar propagation delay	τ_{PDE}	Pull up ISET from 0V to 1V	5	20	40	µs
PG low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull up to 3.3V through a 100kΩ resistor		500	800	mV
	V_{OL_10}	V_{IN} = 0V, pull up to 3.3V through a 10kΩ resistor		600	800	mV

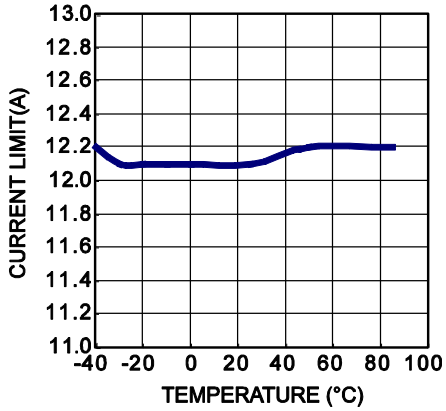
Notes:

4) Guaranteed by over-temperature correlation, and not tested in production.
5) Guaranteed by design.

TYPICAL CHARACTERISTICS

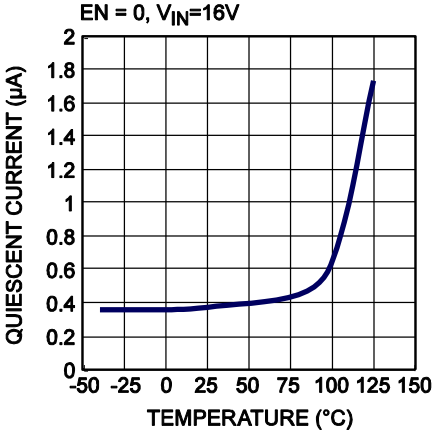
V_{IN} = 12V, C_{OUT} = 220µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 10kΩ, T_A = +25°C, unless otherwise noted.

Current Limit vs. Temperature



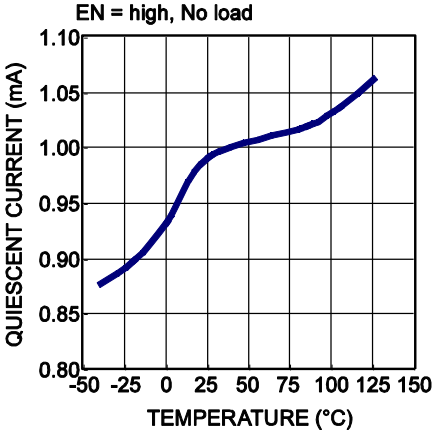
Quiescent Current vs. Temperature

EN = 0, V_{IN}=16V

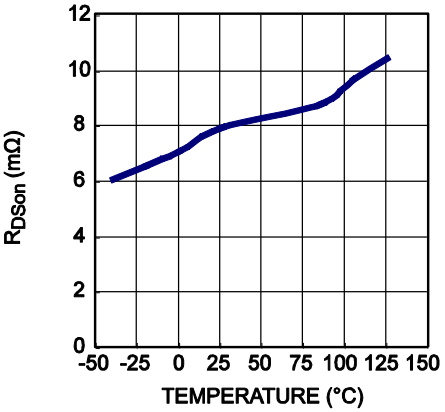


Quiescent Current vs. Temperature

EN = high, No load

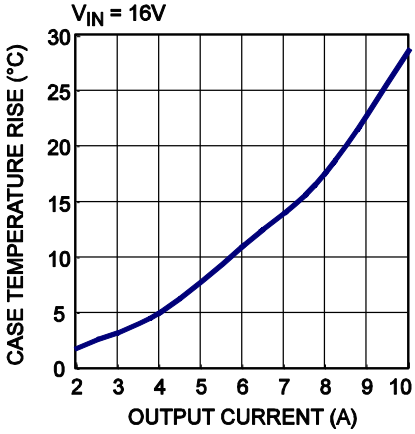


R_{DSon} vs.Temperature



Case Temperature Rise vs. Output Current

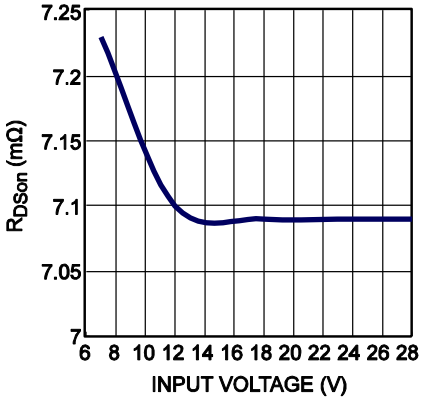
V_{IN} = 16V



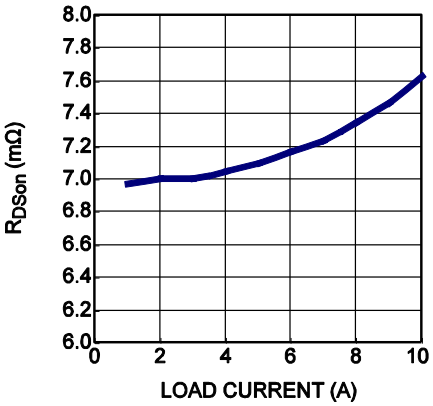
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, C_{OUT} = 220µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 10kΩ, T_A = +25°C, unless otherwise noted.

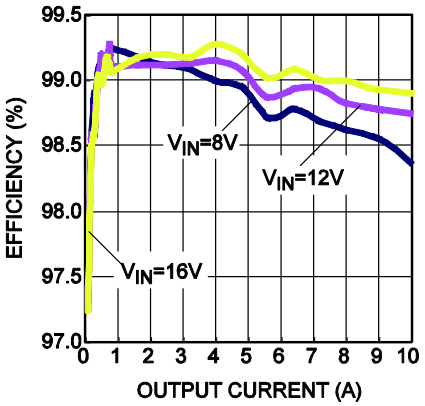
R_{DSon} vs. Input Voltage



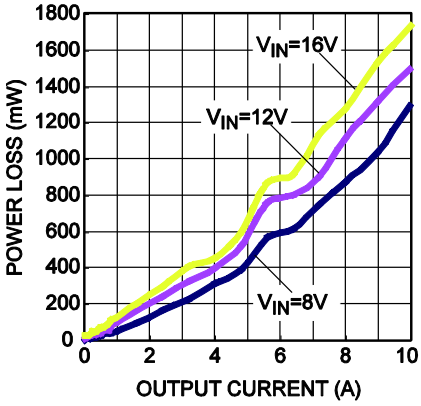
R_{DSon} vs. Load Current



Efficiency vs. Load Current



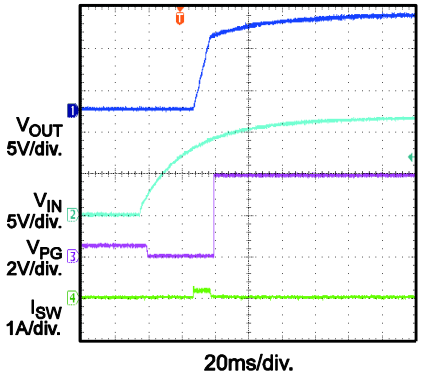
Power Loss vs. Load Current



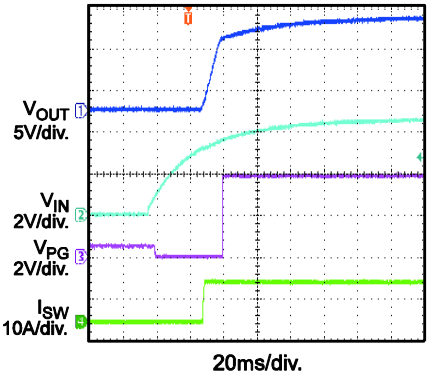
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, C_{OUT} = 220µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 10kΩ, T_A = +25°C, unless otherwise noted.

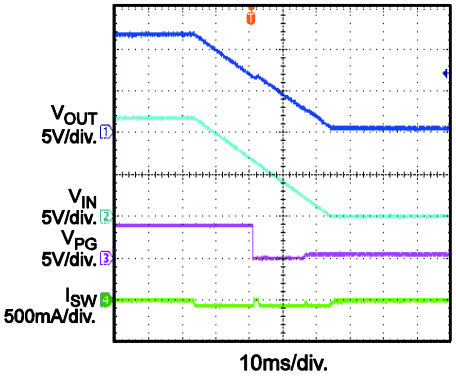
Start-Up through VIN
I_{OUT} = 0A



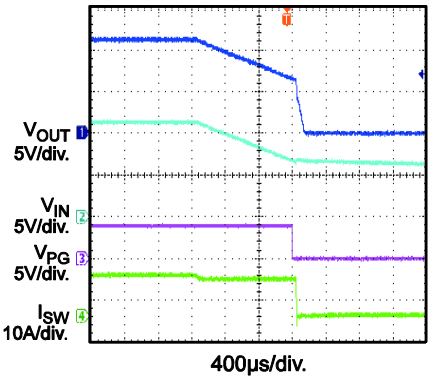
Start-Up through VIN
I_{OUT} = 10A



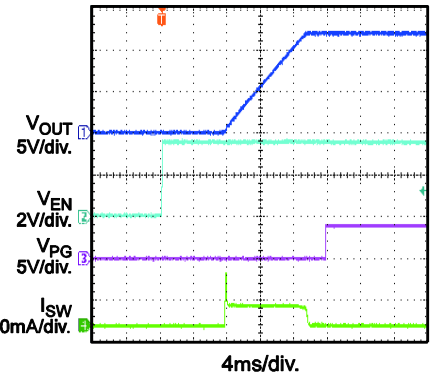
Shutdown through VIN
I_{OUT} = 0A



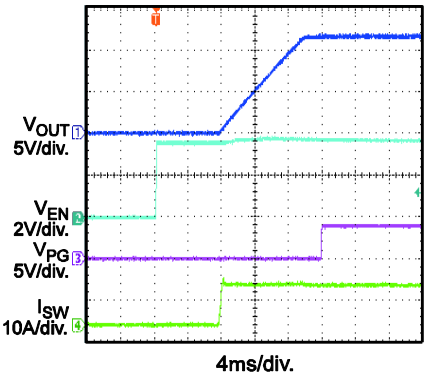
Shutdown through VIN
I_{OUT} = 10A



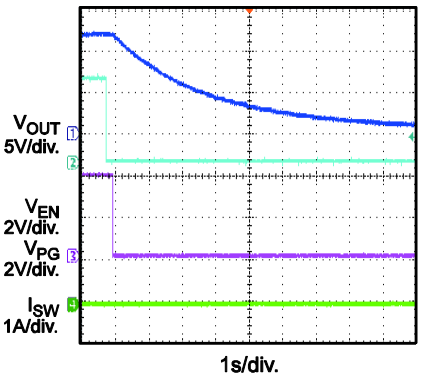
Start-Up through EN
I_{OUT} = 0A



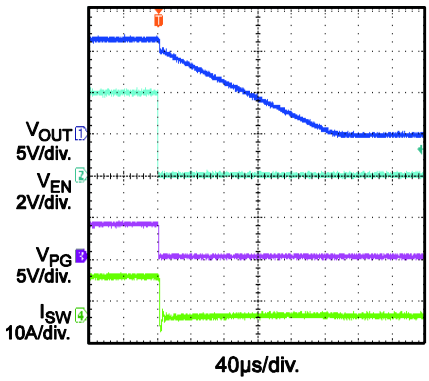
Start-Up through EN
I_{OUT} = 10A



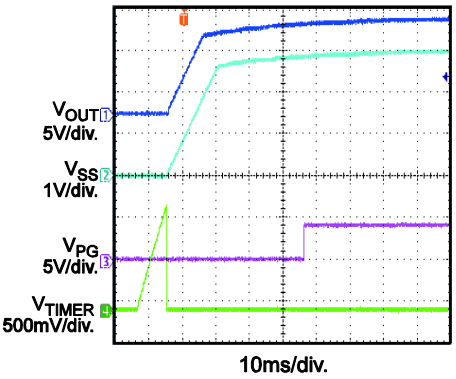
Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 10A



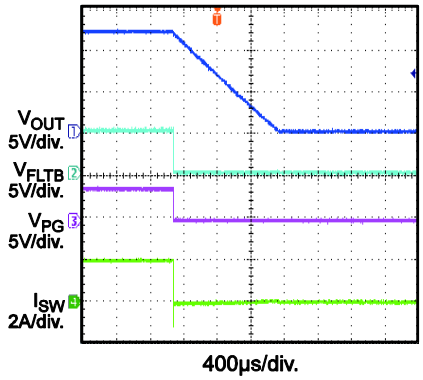
Start-Up Sequence



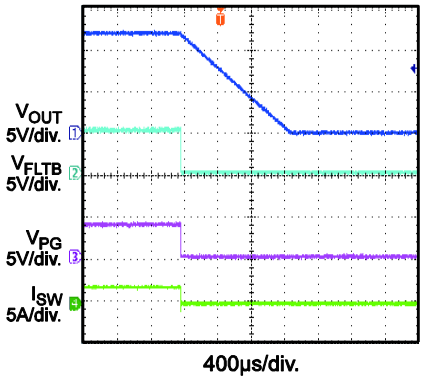
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, C_{OUT} = 220µF, C_T = 220nF, C_{SS} = 47nF, R_{SET} = 10kΩ, T_A = +25°C, unless otherwise noted.

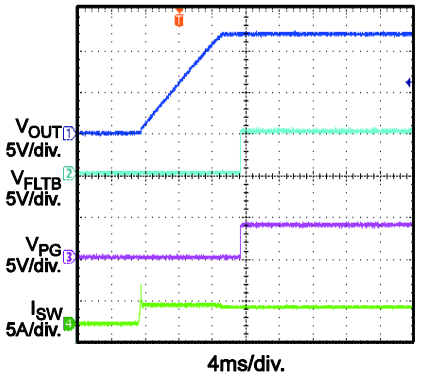
Thermal Shutdown
I_{OUT} = 2A, latch mode



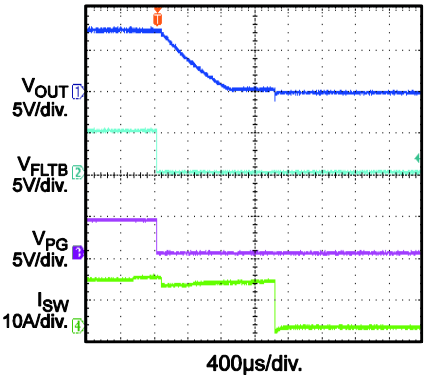
Thermal Shutdown
I_{OUT} = 2A, retry mode



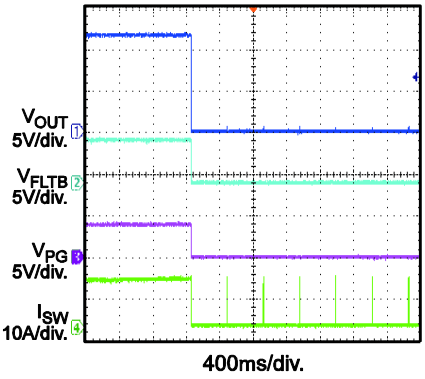
Thermal Recovery
I_{OUT} = 2A, retry mode



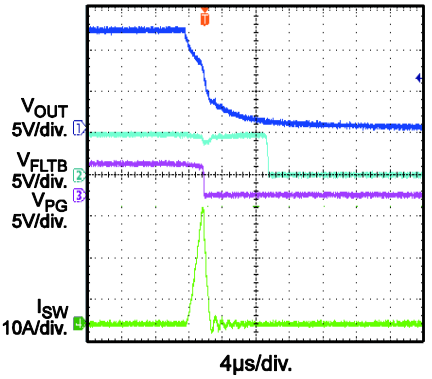
OCP
V_{IN} = 12V, latch mode



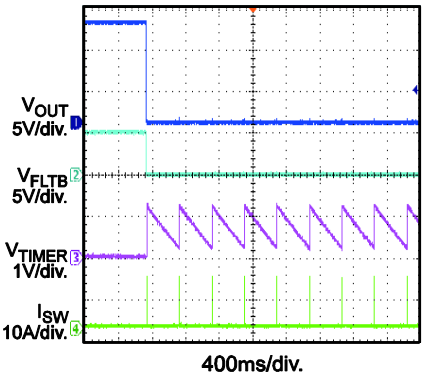
OCP
V_{IN} = 12V, retry mode



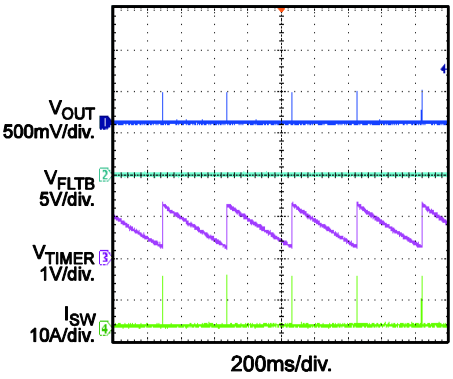
SCP Entry
V_{IN} = 12V, latch mode



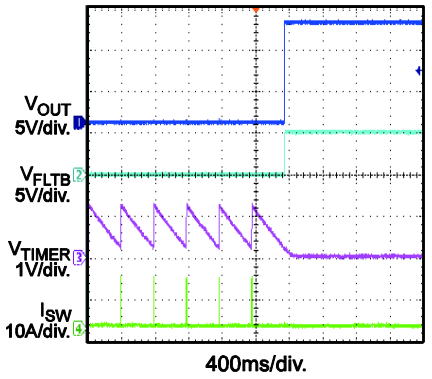
SCP Entry
V_{IN} = 12V, retry mode



SCP Steady State
V_{IN} = 12V, retry mode



SCP Recovery
V_{IN} = 12V, retry mode



FUNCTIONAL BLOCK DIAGRAM

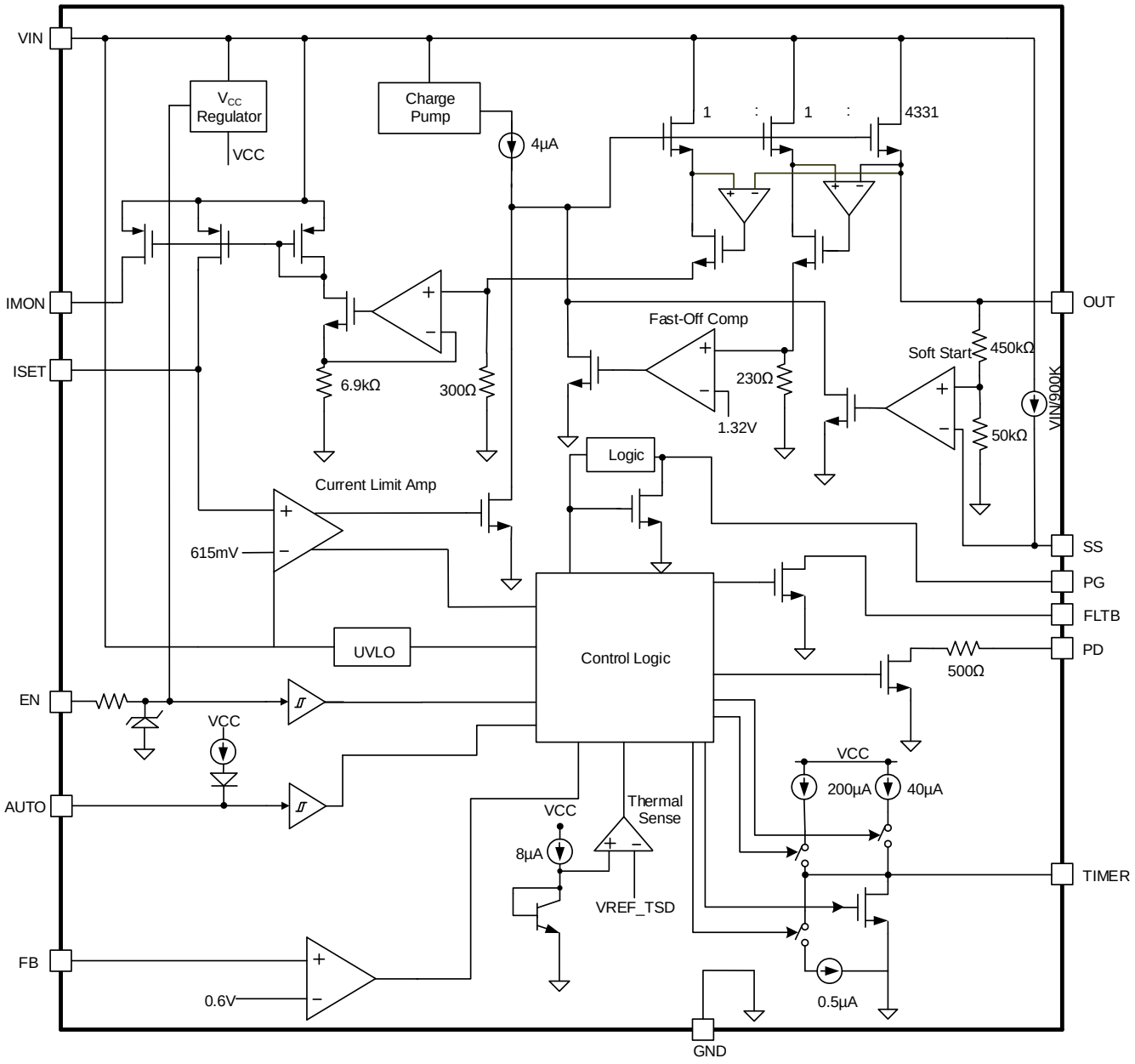


Figure 1: Functional Block Diagram

OPERATION

The MP5061 limits the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop and the dV/dt of the voltage to the load. The part provides an integrated solution to monitor the input voltage, output voltage, output current, and die temperature to eliminate the need for an external current-sense power resistor, power MOSFET, and thermal sense device.

Current Limit

The MP5061 provides a constant current limit that can be programmed by an external resistor. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. In order to limit the current, the gate-to-source voltage needs to drop from 5V to about 1V. The typical response time is about 20µs, and the output current may have a small overshoot during this time period.

When the current limit triggers, the fault timer starts. If the output current falls below the current limit threshold before the end of the fault timeout period, the MP5061 resumes normal operation. If the current limit duration exceeds the fault timeout period, the power FET turns off. The subsequent behavior relates to the AUTO pin configuration. If the temperature reaches the thermal protection threshold during the fault timeout period, the power FET turns off.

When AUTO is floating, the part functions in auto-retry mode for over-current protection. The part enters latch-off mode when AUTO pulls to ground (once it detects an over-current condition) and the duration exceeds the preset value.

If the device reaches either its current limit or its over-temperature threshold, the FLTB pin is driven low with a 21µs propagation delay to indicate a fault. The desired current limit at normal operation is a function of the external current-limit resistor.

Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold significantly before the control loop can respond. If the current reaches a 25A secondary current limit level, a fast turn-off circuit activates to turn off the power FET using a 100mA pull-down gate discharge current (see Figure 2). This limits the peak current through the switch to limit the input voltage drop. The total short-circuit response time is about 200ns. FLTB switches low once it reaches the 25A current limit, and asserts low until the circuit resumes normal operation levels.

Fault Timer and Restart

When the current reaches its over-current limit threshold, a 200µA fault timer current source charges the external capacitor (C_T) at the TIMER pin. If the current-limit state ceases before TIMER reaches 1.23V, the MP5061 returns to normal operation mode and a low-value resistor discharges C_T after the TIMER voltage reaches 1.23V. If the current-limit state continues after the TIMER voltage reaches 1.23V, the power FET switches off. The subsequent restart procedure then depends on the selected retry configuration.

If the AUTO pin connects to ground or low, the MP5061 latches off. Restart the input power or cycle the EN signal to resume operation.

Floating AUTO causes the device to work in hiccup mode (see Figure 3). At the end of the fault timeout period, the power switch turns off, and a low current sink of 0.5µA discharges C_T.

When the TIMER voltage reaches the low threshold (0.2V), the part restarts. If the fault condition remains, the fault timeout period and restart timer repeat.

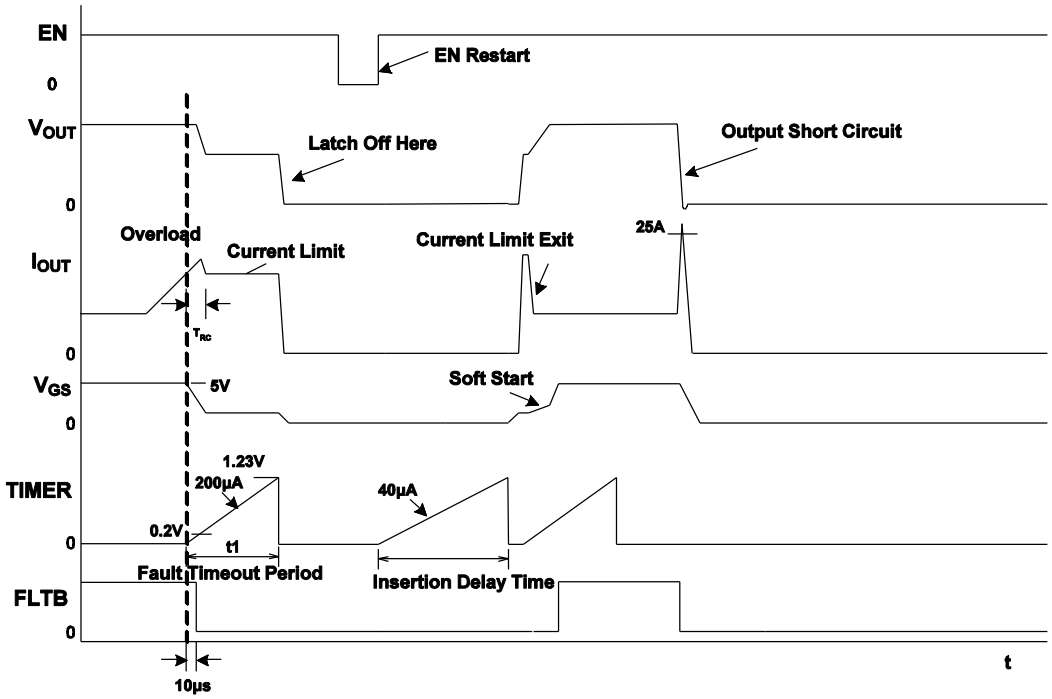


Figure 2: Over-Current Protection (Latch-Off Mode, AUTO = Low)

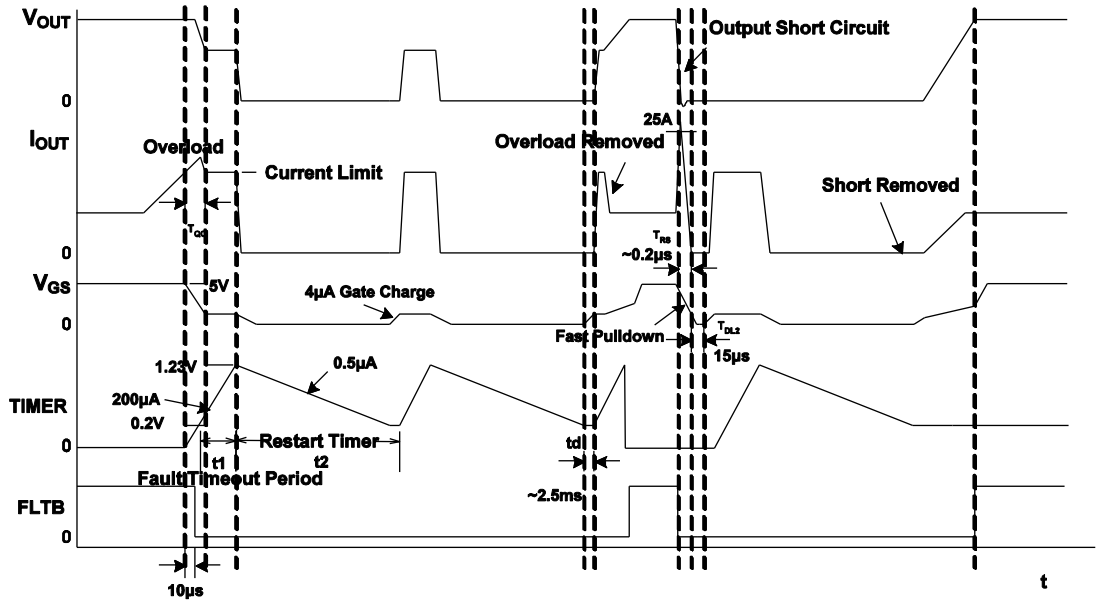


Figure 3: Over-Current Protection (Auto-Retry Mode, AUTO = High)

Power Good

The PG pin indicates whether the output voltage is in the normal range relative to the input voltage, and is the open drain of a FET. Pull up PG to the external power supply through a 100kΩ resistor. During power-up, the PG output is driven low. This directs the system to remain off and minimize the OUT load to reduce inrush current and power dissipation during start-up.

The power-good signal is pulled high when the device reaches any of the following conditions:

- V_{FB} > 0.6V
- V_{GS} > 3V
- V_{OUT} > V_{IN} - 1V

The system can then draw full power.

If the FB voltage drops below 0.535V, the power FET's V_{GS} voltage is less than 3V, or the output voltage is less than V_{IN} - 1V, PG is switched low.

The PG output is pulled low if the EN pin is below its threshold or the input UVLO is triggered.

With no input, PG stays at a logic low level in the presence of a pull-up supply.

FLTB Pin

The fault bar (FLTB) pin is an open-drain output used to indicate that a fault has occurred. Pull up the FLTB pin to an external power supply through a 100kΩ resistor.

If the device reaches its current limit, the die temperature exceeds the thermal shutdown threshold, or the MOSFET is shorted before power-up, the fault output is driven low with a 21µs propagation delay. If a short occurs and the current reaches its 25A secondary current limit, FLTB switches low with an ~8µs delay.

FLTB goes high when the MP5061 resumes normal operation, which means the output voltage exceeds the setting voltage of the PG rising threshold and power FET is fully on (V_{GS} > 3V).

External Pull-Up Voltage for PG and FLTB

PG and FLTB need an external power supply. The open-drain output of PG can work well from the external pull-up voltage even when V_{IN} = 0 and EN is disabled. Use a 100kΩ pull-up resistor for PG and FLTB.

Power-Up Sequence

For hot-swap applications, the input of the MP5061 can experience a voltage spike or transient during the hot-plug procedure. This spike is caused by the parasitic inductance of the input trace and the input capacitor. An insertion delay determined by the external capacitor at the TIMER pin stabilizes the input voltage.

Figure 4 shows that the input voltage rises immediately, and a 30Ω resistor pulls the internal V_{GS} voltage low.

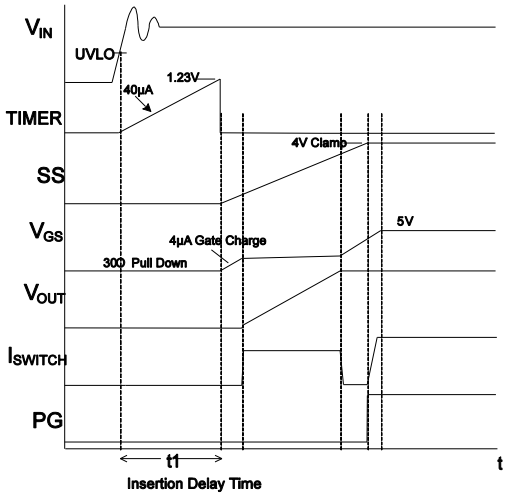


Figure 4: Start-Up Sequence

TIMER charges through a 40µA constant-current source when the input voltage reaches the UVLO threshold. When the TIMER voltage reaches 1.23V, a 4µA current source pulls up the power FET's gate-source voltage. Meanwhile, the TIMER voltage drops. Once the gate voltage reaches its threshold (V_{GSTH}), the output voltage rises. The soft-start capacitor determines the rise time.

Soft Start

A capacitor connected to the SS pin determines the soft-start time. When the insertion delay time ends, a constant-current source proportional to the input voltage ramps up the voltage on SS. The output voltage rises at a similar slew rate to the SS voltage.

The SS capacitor value is determined with Equation (1):

$$C_{SS} = \frac{10 \cdot \tau_{SS}}{R_{SS}} \quad (1)$$

Where τ_{SS} is the soft-start time and R_{SS} = 2MΩ. For example, a 100nF capacitor gives a soft-start time of 20ms.

If the load capacitance is extremely large, the current required to maintain the preset soft-start time will exceed the current limit. Then, the load capacitor and the current limit control the rise time.

Float SS to generate a fast ramp-up voltage. A 4μA current source pulls up the gate of the power FET. The gate-charge current controls the output voltage rise time. The approximate soft-start time is about 1ms, which is the minimum soft-start time.

Enable Pin

When the voltage is higher than the EN pin's rising threshold, it enables the part. When the voltage is lower than the threshold, it disables the part.

When EN < 0.6V, the chip goes into the lowest shutdown-current mode. When EN is higher than 0.6V but lower than its rising threshold, the chip remains in shutdown mode with a slightly larger current.

When EN enables the part, the insertion delay timer starts. When the insertion delay time ends, the internal 4μA current source charges the power FET's gate. Charging typically takes about 1.5ms to reach the V_{GS} threshold. Then, the output voltage rises following the SS-controlled slew rate.

Damaged MOSFET Detection

The MP5061 can detect a shorted pass FET during power-up by treating an output voltage that exceeds V_{IN} - 1V during power-up as a short on the MOSFET. The FLTB pin goes low to indicate a fault condition, and the power switch remains off. Once $V_{OUT} \leq V_{IN}$ - 1, the part starts up normally.

Internal VCC Sub-Regulator

The MP5061 has an internal, 5V, linear sub-regulator that powers low-voltage circuitry. This regulator takes input voltage and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. Lower V_{IN} values result in lower output voltages. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

PD Pin

When the PD pin connects to the output, the part is in pull-down mode. In this mode, when V_{IN} is lower than its UVLO or EN is between 0.6V and the rising threshold, an integrated 500Ω pull-down resistor attached to the output discharges the output. Adding a resistor between PD and the output results in a slower output drop. If PD is floating, pull-down mode is disabled.

AUTO Pin

When the AUTO pin is floating, the MP5061 is in auto-retry mode. In auto-retry mode, the part turns off when it exceeds its thermal limit or current limit timeout, and turns back on when the part cools by 28°C or the restart timer completes.

When the AUTO pin is tied to ground, the part is in latched-fault mode. In latched-fault mode, a thermal fault or current-limit fault latches the output off until the enable line is toggled from low to high or the input voltage restarts.

Under-Voltage Lockout

If the input supply falls below the UVLO threshold, the output is disabled and the PG pin goes low.

When the supply exceeds the UVLO threshold, the output is enabled and the PG line is released.

Monitoring the Output Current

The IMON pin provides a voltage proportional to the output current (the current through the power device). Place a resistor to ground to set the gain of the output. Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.

APPLICATION INFORMATION

Setting the Current Limit (R_{SET})

The MP5061 current-limit value should exceed the normal maximum load current, allowing the tolerances in the current-sense value. Estimate the current limit using Equation (2):

$$I_{limit} = \frac{0.6(V)}{R_{SET}} \times 20 \times 10^4 (A) \quad (2)$$

Table 1 shows the bench results from the evaluation board. Figure 5 shows the relationship between R_{SET} and the current limit.

Table 1: Current Limit vs. Current Limit Resistor

Current Limit Resistor (kΩ)	7.5	10	20
Current Limit (A)	15.9	12.1	6.08

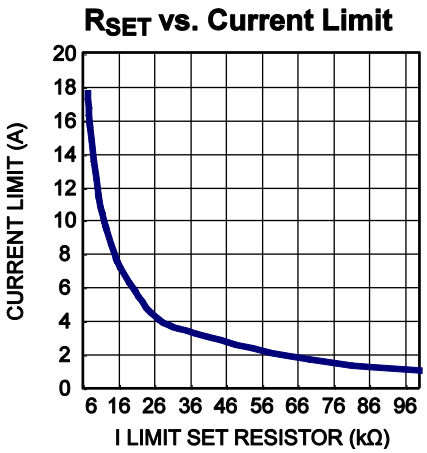


Figure 5: R_{SET} vs. Current Limit

Current Monitor

The MP5061 provides a power MOSFET current monitoring function. Place a resistor (R_{MON}) to ground to set the gain of the output using Equation (3):

$$IIMON = \frac{I_{powerfet}}{10^5} \quad (3)$$

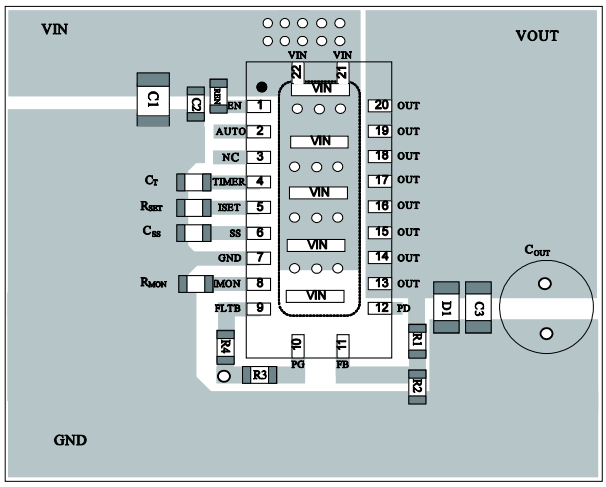
Where $I_{powerfet}$ is the power MOSFET current.

Place a 10kΩ resistor from IMON to GND to get 100mV/A. Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.

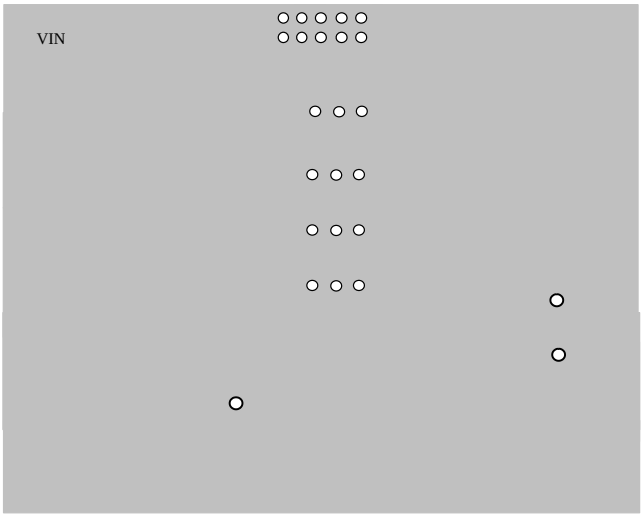
PCB Layout Guidelines

Proper PCB layout is critical for good performance. For best results, refer to Figure 6 and follow the guidelines below:

1. Place the high-current paths (GND, IN, and OUT) very close to the device using short, direct, and wide traces.
2. Place a transient voltage suppressor diode (TVS) as close to VIN as possible. The TVS helps the MP5061 avoid input voltage overshoot when the load current decreases sharply. A small bypass capacitor is recommended to help minimize transients that may occur on the input supply line.
3. Place the external feedback resistors next to the FB pin. Avoid placing any vias on the FB trace.
4. Place the Schottky diode close to the OUT and GND pins. This Schottky diode can limit the V_{OUT} negative excursion at the OUT pin when the load current shuts off.
5. Connect the IN and GND pads to a large copper trace to achieve better thermal performance.
6. Place the input and output capacitors as close to the part as possible to minimize the effect of PCB parasitic inductance.
7. Put vias in the thermal pad and provide a large copper area near the IN pin to improve thermal performance. Ensure that all pins are connected to get equal current distribution in all legs. The same process is recommended for all OUT pins.



Top Layer



Bottom Layer

Figure 6: PCB Layout

Design Example

Figure 7 shows the detailed application schematic. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 9. For more detailed device applications, refer to the related Evaluation Board Datasheets for the MP5061.

TYPICAL APPLICATION

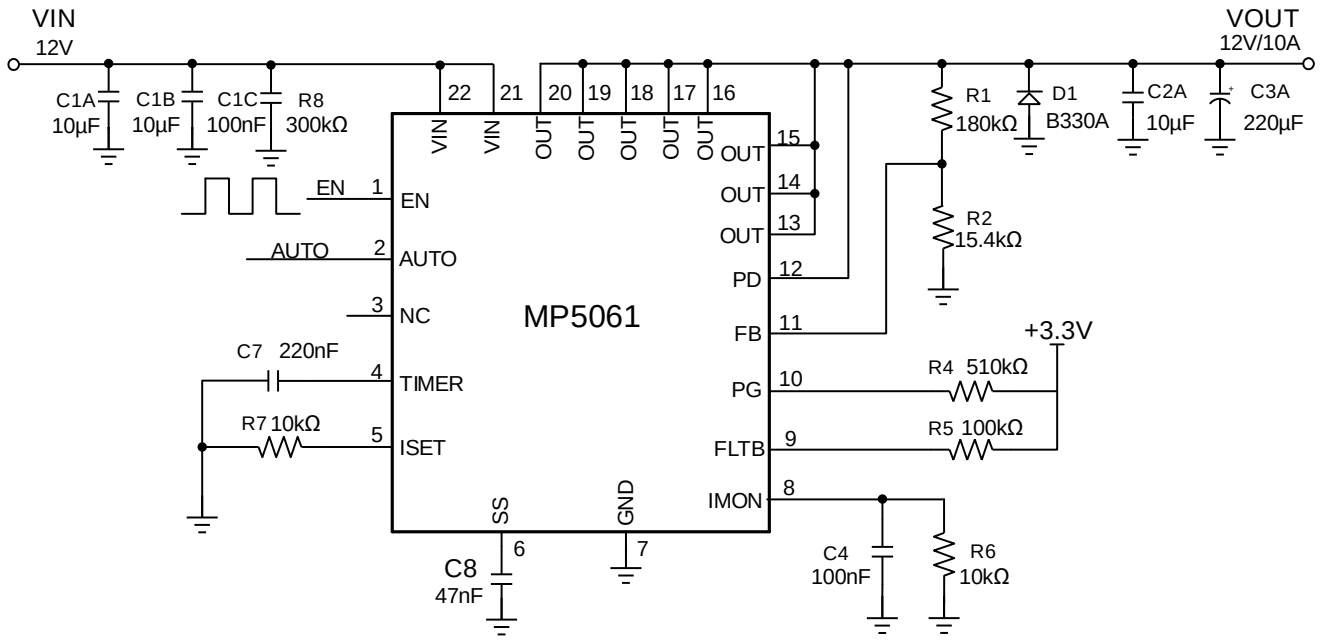
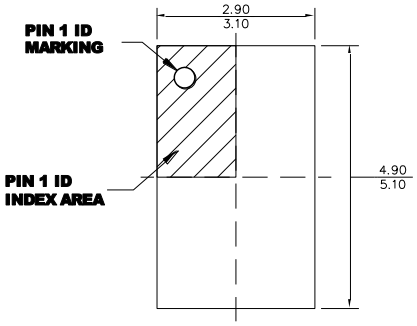


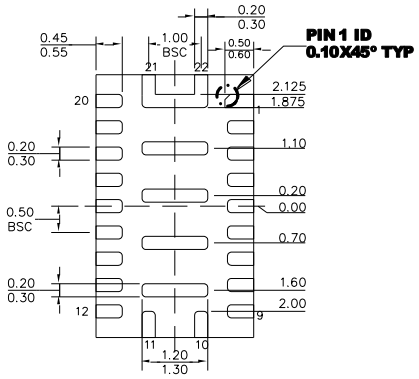
Figure 7: Typical Application Circuit with 10ms Soft-Start Time, 12A Current Limit

PACKAGE INFORMATION

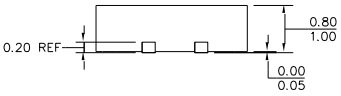
QFN-22 (3mmx5mm)



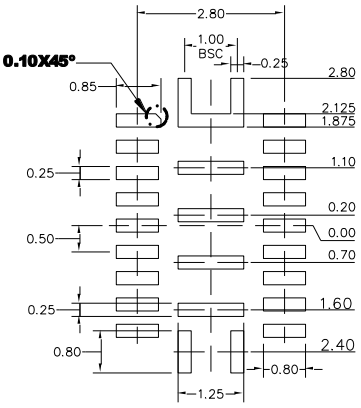
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.